ABSTRACT:

The present invention describes an integrated circuit (100) having a processor that consists of a plurality of identical, or at least very similar, processing elements (120) organized in a regular grid. Each processing element (120) is capable of executing the desired functionality of the processor. The processing elements (120) are interconnected by a configurable interconnection network (140) and are controlled by a program sequencing issuing device (160) capable of handling exceptions in the instruction flow through the processing elements (120). Consequently, the integrated circuit (100) can be easily redesigned, thus reducing design effort and time-to-market for such architectures.

Fig. 1